REMARKS

Claims 4-13, 18, 19, 21-24, 31-42, 44-46, 51-71, and 74-76 remain pending in this application and claims 21, 31, 32, 39, 42, 46, 56, 61, 62, 68, and 76 are amended herein. Support for the amendments may be found throughout the Specification, at least in Fig. 3 and related text and in the originally filed claims.

Objections to application and reissue declaration

The instant application is objected to under 37 C.F.R. § 1.172(a) as lacking the written consent of all assignees owning an undivided interest in the patent. Applicants hereby submit the Statement Establishing Right of Assignee to Prosecute attached hereto and request that the objection to the application be withdrawn.

The reissue oath/declaration is objected to because the error which is relied upon to support the reissue application is not an error upon which a reissue can be based, and because it does not state that the inventor is the "original and first inventor." Applicants respectfully submit that the supplemental oath/declaration submitted herewith addresses these objections.

Objection to the Specification

In the Office action mailed on July 21, 2006, the Examiner required submission of a substitute Specification due to typographical errors in the one originally filed. Applicants submit that the marked-up and clean versions of the Specification attached hereto satisfy this requirement. The Specification has been amended to correct obvious typographical errors; no new matter has been added.

Objections to Claims

Claims 39, 42, 56, 61, 62, and 68 are objected to for informalities. Applicants respectfully submit that the foregoing amendments fully address the objections to these claims.

Rejections for Double Patenting

Claims 4-13, 18, 19, 21-24, 31-42, 44-46, 51-71, and 74-76 stand rejected under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims of commonly-owned U.S. Patent No. 5,673,218. Claims 31-35 further stand rejected

under the judicially-created doctrine of obviousness-type double patenting as being unpatentable over claims of commonly-owned U.S. Patent No. 6,956,757. Applicants respectfully note that these rejections are overcome by the two Terminal Disclaimers submitted herewith along with a check to cover the requisite fee.

Rejection of Claims under 35 U.S.C. § 112

Claims 4-13, 18, 19, 21-24, 31-42, 44-46, 51-71, and 74-76 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The following chart includes non-limiting illustrative examples of the claim elements in question. Also, the foregoing claim amendments fully address the double inclusion of elements raised by the Examiner.

Element/Feature	***Illustrative Example***
First and second sets of conductive address lines	Fig. 3, elements O and P
Series of information-defining nonlinear elements	Fig. 3, element K
Address circuitry	Fig. 3, elements L and N
Sensing circuitry	Fig. 3, element U
Additional address circuitry	Fig. 3, elements Q and T
Threshold activation voltage	Fig. 12, element F
First set of selectable disabling lines	Fig. 3, element N
First pattern of nonlinear elements	Fig. 3, element L
Circuitry for applying a third voltage	Fig. 4, elements V and X
Second set of selectable disabling lines	Fig. 3, element Q
Second pattern of nonlinear elements	Fig. 3, element T
Circuitry for applying a fourth voltage	Fig. 4, elements W and Y
Output line	Fig. 3, element M

Sensing nonlinear element	Fig. 3, element U
First series of voltage-drop elements	Fig. 3, element R
Circuitry for applying a first voltage	Fig. 1, element A
Second series of voltage-drop elements	Fig. 3, element S
Circuitry for applying a second voltage	Fig. 1, element A
Circuitry that is external to the information-storagecircuit for biasing the rectifiers	Fig. 1, element A

Rejection of Claims under 35 U.S.C. § 102

Claims 4-7, 11-13, 18, 19, 21, 31-36, 40, 42, and 69-71 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 4,070,654 to Tachi ("Tachi"). Tachi appears to disclose a read-only memory array addressed by bipolar transistors. The Examiner relies on Tachi to teach all of the limitations of independent claim 31. Tachi does not, however, disclose address circuitry for disabling all but a selected one of a first set of address lines. Rather, Tachi's address circuitry operates by enabling an entire set of address lines when voltage is applied to the base of a selected input transistor, i.e., all digit output lines intersecting a given selection input line are read in parallel. *See* Tachi, column 2, line 47 to column 3, line 4. In contrast, the instant claims require address circuitry for disabling all but one of a selected set of address rows or columns. Moreover, Tachi does not disclose address circuitry comprising a first pattern of rectifiers connected directly to a first set of address lines, as recited in amended claim 31. Rather, Tachi's address lines are connected directly to selection input transistors and digit output transistors. *See* Tachi, Fig. 1 and related text. Applicants submit that amended independent claim 31 and claims dependent therefrom are allowable for at least these reasons.

Claims 4-7, 11-13, 18, 19, 21, 22, 31-42, 44-46, and 51-71 also stand rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 4,347,585 to Eardley ("Eardley"). Eardley appears to disclose a Schottky diode-based storage matrix. The Examiner relies on Eardley to teach all of the limitations of independent claim 31. Eardley does not, however, disclose address circuitry for disabling all but a selected one of a first set of address lines, as required by the present claims. Rather, Eardley's address circuitry operates by enabling a

selected address line by raising a potential. *See* Eardley, column 4, lines 43-47. Moreover, Eardley does not disclose address circuitry comprising a first pattern of rectifiers connected directly to a first set of address lines, as recited in amended claim 31. Rather, Eardley's address lines are connected directly to transistor-based driver circuitry. *See* Eardley, Figs. 3 and 4 and related text. Applicants submit that amended independent claim 31 and claims dependent therefrom are allowable for at least these reasons.

Claims 4-7, 11-13, 18, 19, 21, 22, 31-42, 44-46, and 51-71 also stand rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 4,661,927 to Graebel ("Graebel"). Graebel appears to disclose a Schottky logic read only memory. The Examiner relies on Graebel to teach all of the limitations of independent claim 31. Graebel does not, however, disclose address circuitry comprising a first pattern of rectifiers connected directly to a first set of address lines, as recited in amended claim 31. Rather, Graebel's address lines are connected directly to drivers including NPN and PNP transistors. *See* Graebel, column 4, lines 23-28. Applicants submit that amended independent claim 31 and claims dependent therefrom are allowable for at least this reason.

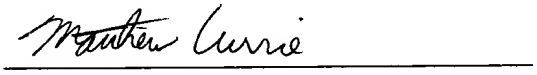
CONCLUSION

In light of the foregoing, Applicants respectfully submit that all claims are now in condition for allowance.

A petition for a one-month extension of time and a check for $190 for the extension of time fee and the two Terminal Disclaimer fees are enclosed. Applicants believe that no additional fees are necessitated by the present Response. However, in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Deposit Account No. 07-1700.

If the Examiner believes that a telephone conversation with Applicants' agent would expedite allowance of this application, the Examiner is cordially invited to call the undersigned agent at (617) 570-1198.

Respectfully submitted,



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